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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, KHIEM D	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 04/10/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)	
Office Action Summary	09/742,204	FOX ET AL.	
	Examin r	Art Unit	
	Khiem D Nguyen	2823	

-- Th MAILING DATE of this communication app ars on the cover sh t with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) *25 and 26* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20 and 22-24* is/are rejected.

7)☒ Claim(s) *21* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

   (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Evans et al. (U.S. Patent 6,150,184).

   AAPA teaches a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of (see the Background of the Invention on pages 1-4 of this application):

   deposition of an electrically conductive bottom electrode layer;

   deposition of a layer of ferroelectric dielectric material, wherein the ferroelectric dielectric layer is comprises PZT;

   annealing the layer of ferroelectric dielectric material with a first anneal;

   annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed by rapid thermal annealing; and

   deposition of an electrically conductive top electrode layer.

AAPA teaches doing the rapid thermal annealing before the formation of the top electrode but fails to teach doing the rapid thermal annealing after the formation of the top electrode as recited in present claims 1.

However, ***it would have been obvious to one of ordinary skill in the art*** to perform the rapid thermal annealing after the formation of the top electrode because selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

Alternatively, Evans teaches a second anneal being performed after the step of deposition of an electrically conductive top electrodes layer. See Fig. 11 and col. 7, lines 48-56. ***It would have been obvious to one of ordinary skill in the art*** to perform the rapid thermal annealing after the formation of the top electrode because in doing so the electrical switching of the ferroelectric capacitors are improved. See col. 2, lines 1-7.

3. Claims 2,3, 5, 6, 7, 8, 9, 10, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Evans et al. (U.S. Patent 6,150,184) as applied to claims 1 and 4 above, and further in view of Joshi et al. (U.S. Patent 6,322,849) and Van Buskirk et al. (U.S. Patent 6,316,797).

AAPA fails to teach that the electrically conductive bottom electrode layer comprises a noble metal and wherein the electrically conductive bottom electrode layer comprises platinum as recited in claims 2 and 3.

However, Joshi teaches that the electrically conductive bottom electrode layer comprises platinum and palladium. See col. 5, lines 11-15. ***It would have been obvious***

to one of ordinary skill in the art to use platinum as bottom electrode material in the method of AAPA because platinum can provide electrode or contact function.

AAPA fails to teach that the electrically conductive top electrode layer comprises a noble metal oxide and wherein the electrically conductive top electrode layer comprises iridium oxide as recited in present claims 5 and 6.

However, Van Buskirk teaches that top electrode comprises of iridium oxide. See col. 21, lines 5-10. ***It would have been obvious to one of ordinary skill in the art*** to use iridium oxide as top electrode material in the method of AAPA because iridium oxide can provide electrode or contact function.

AAPA teaches the first annealing is done at a temperature and for time duration but fails to teach the ranges for the annealing temperature and time duration as recited in present claims 7 and 8.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal ranges for the annealing temperature and time duration through routine experimentation and optimization to obtain optimal or desired device performance because the annealing temperature and time duration are result-effective variables and there is no evidence indicating that the annealing temperature and time duration are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

AAPA teaches the second annealing is done at a temperature and for time duration but fails to teach the ranges for the annealing temperature and time duration as recited in present claims 9, 10, and 11.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal ranges for the annealing temperature and time duration through routine experimentation and optimization to obtain optimal or desired device performance because the annealing temperature and time duration are result-effective variables and there is no evidence indicating that the annealing temperature and time duration are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

4. Claims 12, 13, 14, 15, 16, 23, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Evans et al. (U.S. Patent 6,150,184), Joshi et al. (U.S. Patent 6,322,849), and Van Buskirk et al. (U.S. Patent 6,316,797).

AAPA teaches a method for fabrication of ferroelectric capacitor elements of an integrated circuit comprising the steps of (see the Background of the Invention on pages 1-4 of this application):

deposition of an electrically conductive bottom electrode layer comprising a noble metal;

deposition of a layer of ferroelectric dielectric material, wherein the ferroelectric dielectric layer is comprises PZT and performed by sputtering;

annealing the layer of ferroelectric dielectric material with a first anneal;

deposition of an electrically conductive top electrode layer comprising a noble metal oxide; and

annealing the layer of ferroelectric dielectric material with a second anneal, the second anneal being performed by rapid thermal annealing and performed after the step of deposition of an electrically conductive top electrode layer.

AAPA teaches doing the rapid thermal annealing before the formation of the top electrode but fails to teach doing the rapid thermal annealing after the step of deposition of an electrically conductive top electrode layer as recited in present claim 12.

However, ***it would have been obvious to one of ordinary skill in the art*** to perform the rapid thermal annealing after the formation of the top electrode because selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

Alternatively, Evans teaches a second anneal being performed after the step of deposition of an electrically conductive top electrodes layer. See Fig. 11 and col. 7, lines 48-56. ***It would have been obvious to one of ordinary skill in the art*** to perform the rapid thermal annealing after the formation of the top electrode because in doing so the electrical switching of the ferroelectric capacitors are improved. See col. 2, lines 1-7.

AAPA fails to teach that the first anneal is performed in an environment comprising oxygen as recited in present claims 15 and 16.

However, Evans teaches that the first anneal is performed in an oxygen atmosphere. See col. 6, lines 37-52. ***It would have been obvious to one of ordinary skill***

in the art to incorporate Evan's teaching into AAPA's method to performed the first anneal in an environment comprising oxygen because doing so the crystallographic order at the interface of the electrode is improve.

AAPA fails to teach the ranges for the partial pressure of oxygen as recited in claims 15 and 16.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal ranges for the partial pressure of oxygen through routine experimentation and optimization to obtain optimal or desired device performance because the partial pressure of oxygen is result-effective variables and there is no evidence indicating that the partial pressure of oxygen is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

5. Claims 17, 18, 19, 20, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over the applicant's admitted prior art (AAPA) of this application in view of Evans et al. (U.S. Patent 6,150,184), Joshi et al. (U.S. Patent 6,322,849), and Van Buskirk et al. (U.S. Patent 6,316,797) as applied to claims 12, 13, 14, 15, 16, 23, and 24 above, and further in view of Hayashi (U.S. Patent 6,362,503) and Otto et al. (U.S. Patent 6,284,712).

AAPA fails to teach that the first anneal is performed in an environment comprising a mixture of oxygen and inert gas as recited in present claims 17 and 20.

However, Otto teaches that the annealing process is performed in an environment comprising a mixture of inert gas and oxygen. See col. 14, lines 59-64. ***It would have***

been obvious to one of ordinary skill in the art to performed the first anneal in an environment comprising a mixture of oxygen and inert gas because doing so the desired total oxygen pressure can be obtained. See col. 14, lines 59-65. AAPA fails to teach that the second anneal is performed in an environment comprising partial pressure of oxygen as recited in present claims 18 and 19.

However, Hayashi teaches that second anneal is performed in an environment comprising oxygen. See col. 12, lines 14-19. ***It would have been obvious to one of ordinary skill in the art*** to performed the second anneal in an environment comprising oxygen because doing so improves the crystallographic order at the interface of the electrode. See col. 12, lines 14-19.

AAPA fails to teach the ranges for the partial pressure of oxygen as recited in present claims 18 and 19.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal ranges for the partial pressure of oxygen through routine experimentation and optimization to obtain optimal or desired device performance because the partial pressure of oxygen is result-effective variables and there is no evidence indicating that the partial pressure of oxygen is critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

AAPA teaches the second annealing is done at a temperature and for time duration but fails to teach the ranges for the annealing temperature and time duration as recited in present claim 22.

However, it would have been obvious to ***one of ordinary skill in the art of making semiconductor devices*** to determine the workable or optimal ranges for the annealing temperature and time duration through routine experimentation and optimization to obtain optimal or desired device performance because the annealing temperature and time duration are result-effective variables and there is no evidence indicating that the annealing temperature and time duration are critical and it has been held that it is not inventive to discover the optimum or workable ranges of a result-effective variable within given prior art conditions by routine experimentation. See MPEP 2144.05.

Allowable Subject Matter

6. Claim 21 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Khiem D Nguyen whose telephone number is (703) 306-0210. The examiner can normally be reached on Monday-Friday (8:00 AM - 5:00 PM). If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for

the organization where this application or proceeding is assigned are (703) 746-4082 for regular communications and (703) 746-4082 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

K.N.

April 1, 2002

LONG PHAM
PRIMARY EXAMINER